REMARKS

In an Office Action dated July 31, 2008, rejected Claims 1-2 and 11-12 under 35 USC §103(a) as being unpatentable over U.S. Patent No.7,111,303 issued to Macchiano et al. ("Macchiano"). The Examiner has rejected Claims 3-10, 13-20 and 31-61 under 35 USC §103(a) as being unpatentable over Macchiano in view of Applicant's Admitted Prior Art ("AAPA").

In this response, Applicant respectfully traverses the rejections. No amendments are presented. Applicant requests reconsideration of Claims 1-20 and 31-61 in view of arguments as set forth in detail in the following remarks.

CLAIM REJECTIONS – 35 U.S.C. § 103

Claims 1-2 and 11-12 were rejected as being unpatentable over Macchiano. Previously, the Examiner had argued that the AAPA discloses the shared physical memory element recited in Claims 1-2 and 11-12. Now, the Examiner is silent as to what is or is not disclosed in the AAPA, apparently conceding that the AAPA does not disclose the shared physical memory element. The Examiner further concedes that Macchiano, also, does not explicitly teach the use of a shared physical memory element (Office Action dated 7/31/2008, Page 3, Para no. 5). Nevertheless, the Examiner argues that "Macchiano does teach the use of internal buffer storage for data transfers on the virtual LAN," and concludes that "[i]t would have been obvious to one of ordinary skill in the art at the time of the invention that internal buffer storage is in fact a shared physical memory element." (Office Action dated 7/31/2008, Page 3, Para no. 5, citing Macchiano, Col. 5, Lines 23-25). Applicant disagrees. The Examiner's statement is fundamentally

flawed. If it were obvious that internal buffer storage of Macchiano is, in fact, a shared physical memory element, then the Examiner should have made a Section 102 argument of anticipation. There is nothing in Macchiano that indicates that the internal buffer storage is a shared physical memory element. Applicant respectfully requests that the Examiner withdraw the rejection of Claims 1-2 and 11-12 for at least this reason.

Claims 3-10, 13-20 and 31-61 were rejected as being unpatentable over Macchiano in view of AAPA. The rejection is based on the same rationale as the rejections of Claims 1-2 and 11-12 – namely, that the internal buffer storage of Macchiano is, in fact, a shared physical memory element. However, as already noted, there is nothing in Macchiano that indicates that the internal buffer storage is a shared physical memory element, and the remaining disclosure in the AAPA does not cure this deficiency in Macchiano. Accordingly, Applicant respectfully requests that the Examiner withdraw the rejection of Claims 2-10, 13-20 and 31-61 for at least this reason.

With regard to the Examiner's additional arguments in support of the rejection of the amended Claims 41-47, Applicant observes that the Examiner is equating the virtual LAN disclosed in Macchiano with the first direct memory access (DMA) buffer recited in the claims, arguing "the virtual LAN is equivalent to a direct memory access buffer in that it acts as a medium to allow the sending and retrieval of transmitted data." (Office Action dated 7/31/2008, Page 12, Para No. 39). Applicant disagrees, and submits that, at the very least, such an argument is overbroad. Accordingly, Applicant submits that Claims 41-47 are patentably distinguishable over the cited and applied art of record, and requests the withdrawal of the rejection of Claims 41-47 for at least this reason.

The Examiner's further argument that the components 181 and 182 in Fig. 1 of the AAPA discloses mapping a receiving memory element to a second direct memory access buffer as recited in Claims 41-47 is also unsupportable. (See Office Action dated 7/31/2008, Page 12, Para No. 41-42). As noted in Applicant's previous response, in the instant application, the description of Fig.1 and elsewhere in the specification makes a clear distinction between *separate* physical memory elements 181 and 182 as illustrated in Fig. 1, and a *shared* physical memory element. There is nothing that would support an argument that the *separate* physical memory elements 181 and 182 as illustrated in Fig. 1, disclose the direct memory access buffers recited in the claims. Accordingly, Applicant submits that Claims 41-47 are patentably distinguishable over the cited and applied art of record, and requests the withdrawal of the rejection of Claims 41-47 for at least this reason.

CONCLUSION

For at least the foregoing reasons, Applicants submit that the rejections have been overcome. Therefore, Claims 1-20 and 31-61 are in condition for allowance and such action is earnestly solicited. The Examiner is respectfully requested to contact the undersigned by telephone if such contact would further the examination of the present application. Please charge any shortages and credit any overcharges to our Deposit Account number 02-2666.

Respectfully submitted,
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